

★★★**READ PRIOR TO USING THE EVALUATION BOARD**★★★

This guide explains how to connect the enclosed evaluation board so that the LITELINK™ II single chip DAA can be evaluated for performance with modems ranging from V.22 and lower to the latest V.90 specification. Please refer to the LITELINK™ II datasheets for further information on the individual LITELINK™ II parts. The evaluation board also contains the CPC5601 programmable driver IC which allows full software programmability for international modem designs.

This box should contain:

- LITELINK™ II Evaluation Board
- 5 Volt Power Cube (Wall Transformer US Only)
- LITELINK™ II (CPC5610) Data sheet
- CPC5601 Data sheet
- CPC5602 Data sheet

If **ANY** parts are missing from this box, please call 1-800-27CLARE for immediate assistance.

## INSTALLING AND USING

To use the LITELINK™ II board, plug the power cube into a wall socket and connect the other end to the 2.5mm power jack provided on the evaluation board. **Note: When using a power supply other than the one supplied in this package (i.e. foreign voltage supply) you must configure your supply so that the center contact of the 2.5mm power connector is the ground lead and the outside contact is +5V. Alternatively, power may be applied directly to TP1 (+5V) and TP1(Gnd). There is no reverse polarity protection.**

To install the LITELINK™ II evaluation board into a modem design, connections should be made between the Transmit, Receive, Off-Hook, Ring, and Caller ID pins of the LITELINK™ II evaluation board and the modem.

The **Transmit (TX+/-)** path is differential and is connected on J1-1 and J1-2 or the P1 BNC connector. Up to a 0dBm input is allowed on these leads. This connection is normally made to the differential transmit leads of the AFE or codec portion of the data pump or full modem chip(set).

The **Receive (RX+/-)** path may be configured for either differential or single ended operation. As shipped, the jumper J6 is connected between J6-1 and J6-2. Under this condition, the differential receive signal is present on both J2 and the P2 BNC connector. It should be

noted that the shield connection of P2 must not be grounded or the signal will be converted to single ended. If a single ended signal is desired, the jumper J6 may be moved to connect J6-2 and J6-3. Most modem chipset manufacturers use single ended receive signals at the connection point between the modem AFE or codec portion of the data pump or chipset and the DAA.

The Tip and Ring connections to the PSTN line (or line simulator) are made through the **RJ11 jack** provided on the LITELINK™ II eval board.

**Off-hook** (active low) control is performed by connecting the modem controller to  $\overline{\text{OH}}$ , J4-1, of the LITELINK™ II eval board. For prolonged periods of Off-hook measurement, the LITELINK™ II eval board provides capability of connecting a wire from  $\overline{\text{OH}}$ , J4-1 to the ground stake adjacent to J6.

The **Ring** output,  $\overline{\text{RING}}$ , J4-2, of the LITELINK™ II eval board, will provide a signal at the ringing cadence (20Hz to 68Hz in North America). This terminal can be connected to a modem microprocessor for ring detection.

The **Caller ID** control,  $\overline{\text{CID}}$ , J4-3, of the LITELINK™ II eval board, is provided for testing the Caller ID functionality of the CPC5610. When  $\overline{\text{CID}}$  is low, the snoop circuit will be coupled to the receive circuit so that the CID information can be received.

## INTERNATIONAL DESIGN USAGE

For international designs, external components will vary depending on the country-specific requirements for V-I slope, current limit, and AC and DC terminations. This evaluation board addresses this issue by using the CPC5601 programmable driver IC. This device can be programmed through the host to switch in up to 6 different networks. As shipped, the evaluation board is configured with the CPC5601 disabled. AC termination is set to 600Ω and current limit set to 45mA. To enable the CPC5601 and allow program control of AC termination and current limit, remove jumper J1. Alternatively, the board may be hard-wired for 120mA current limit by shorting pins 7 and 8 of the CPC5601.

The impedance networks are effected by sending a digital 1 or 0 into the CPC5601 through the DATA-IN terminal (J4-4). DATA-IN is shifted into a register which enables the pin corresponding to that register bit. This is done in an open drain fashion that will switch in the appropriate values such that the effective value seen



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from the LITELINK™ II chip will change. For instance, for current limiting, the board has  $R16=22.1\Omega$ . This sets the current limit to 45mA (see CPC5610 Datasheet), which is the correct value for European maximum loop currents. In North America, the loop current values are set at 125mA maximum which would require a effective  $8.2\Omega$  resistance, and this value is attained by switching in a  $12.1\Omega$  resistor in parallel by enabling Pin 8. This is accomplished by shifting a 1 into bit position 6 in the CPC5610.

See CPC5601 Datasheet for device programming protocol.

CPC5601 bits 1, 2, and 3 switch in values to select the AC termination impedance. For North American operation, a  $600\Omega$  AC termination is required. Select R26,  $290\Omega$ , by programming bit 1 ON. Bits 2 and 3 must be OFF. It must be noted that the device effectively doubles the termination resistance on the board. Thus, a  $300\Omega$  resistance in the application circuit sets the termination impedance seen at the Tip/Ring terminals to  $600\Omega$ . In addition, if the CPC5601 is used to set the termination

impedance, the series resistance of it's must be considered. In this case, with  $R26=290\Omega$  plus approximately  $10\Omega$  in the CPC5601 output, the circuit will provide the  $600\Omega$  termination to the PSTN line, R28, R29, R30, R31, C15 and C16 are left unpopulated on the PCB to allow use of a customer defined termination network selected by bits 2 and 3.

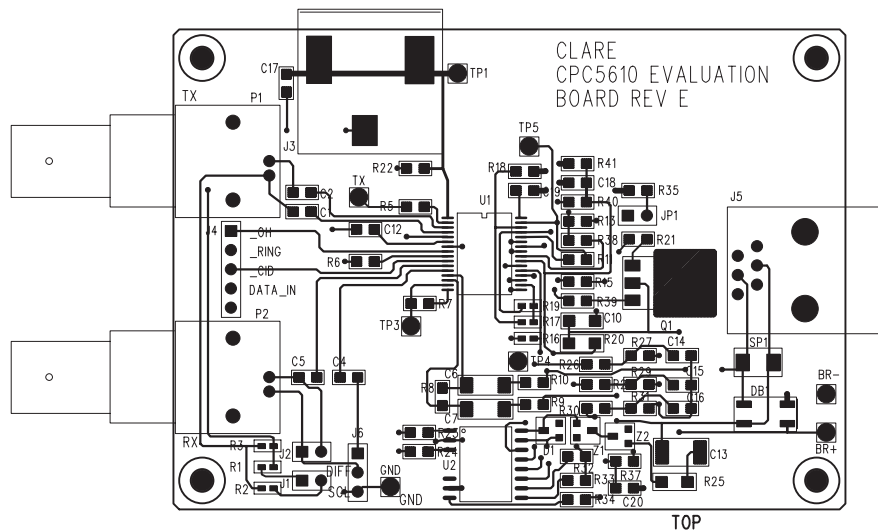
Bits 4 and 5 may be used to modify the VI slope using R32 and R33 (Unpopulated on PCB).

Bit 6 may be used to increase the current limit to approximately 120mA to support North American requirements as defined above.

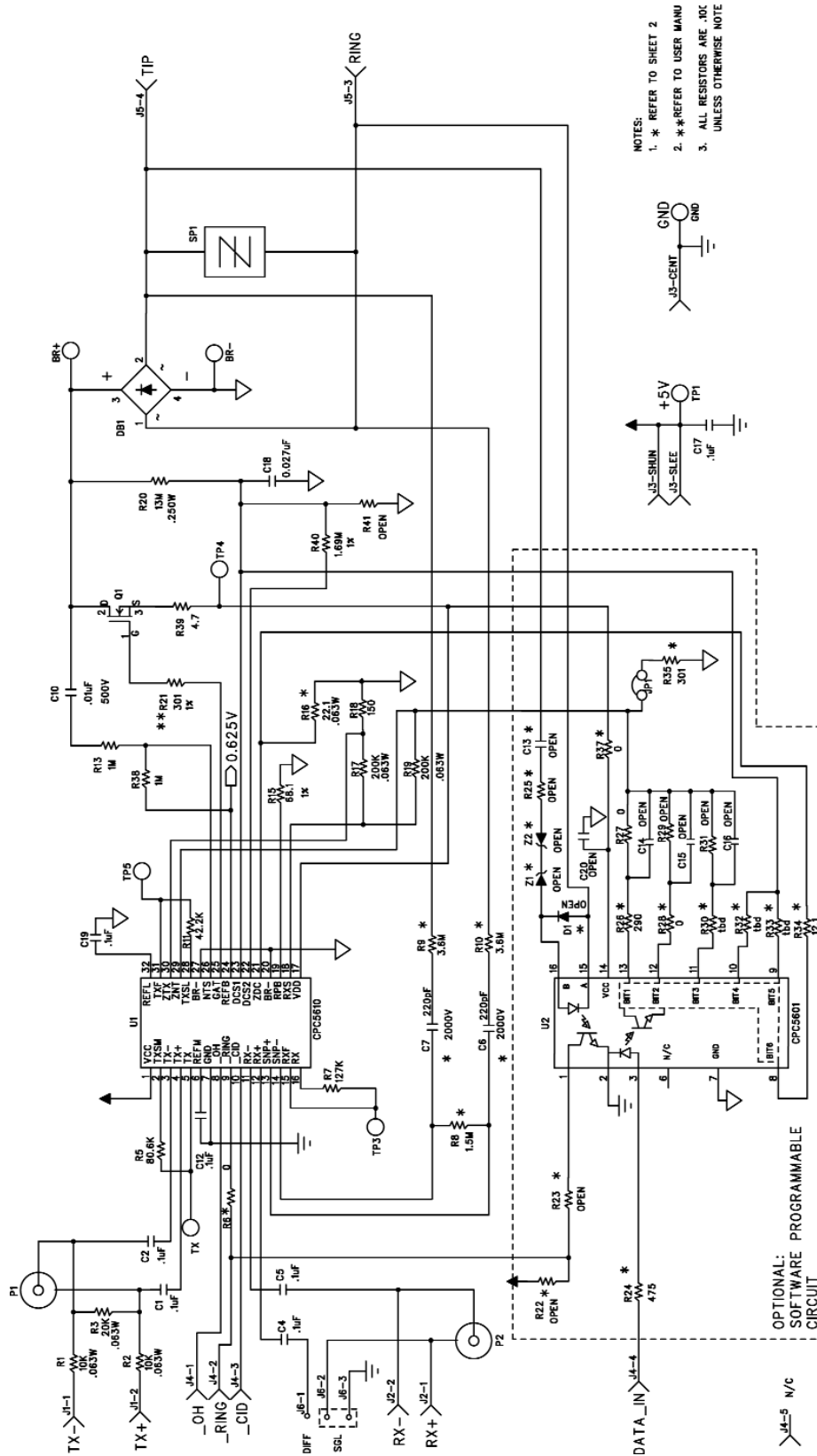
As supplied, the evaluation board is configured to use the snoop circuit for ring detection; however, the PCB provides support for a traditional optocoupler ring detector via the CPC5601 if desired. See the CPC5601 data sheet.

Note: Please add a  $301\Omega$  resistor at R21 for designs with long traces.

## LITELINK™ II Evaluation Board



## LITELINK™ II Evaluation Board Schematic





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