

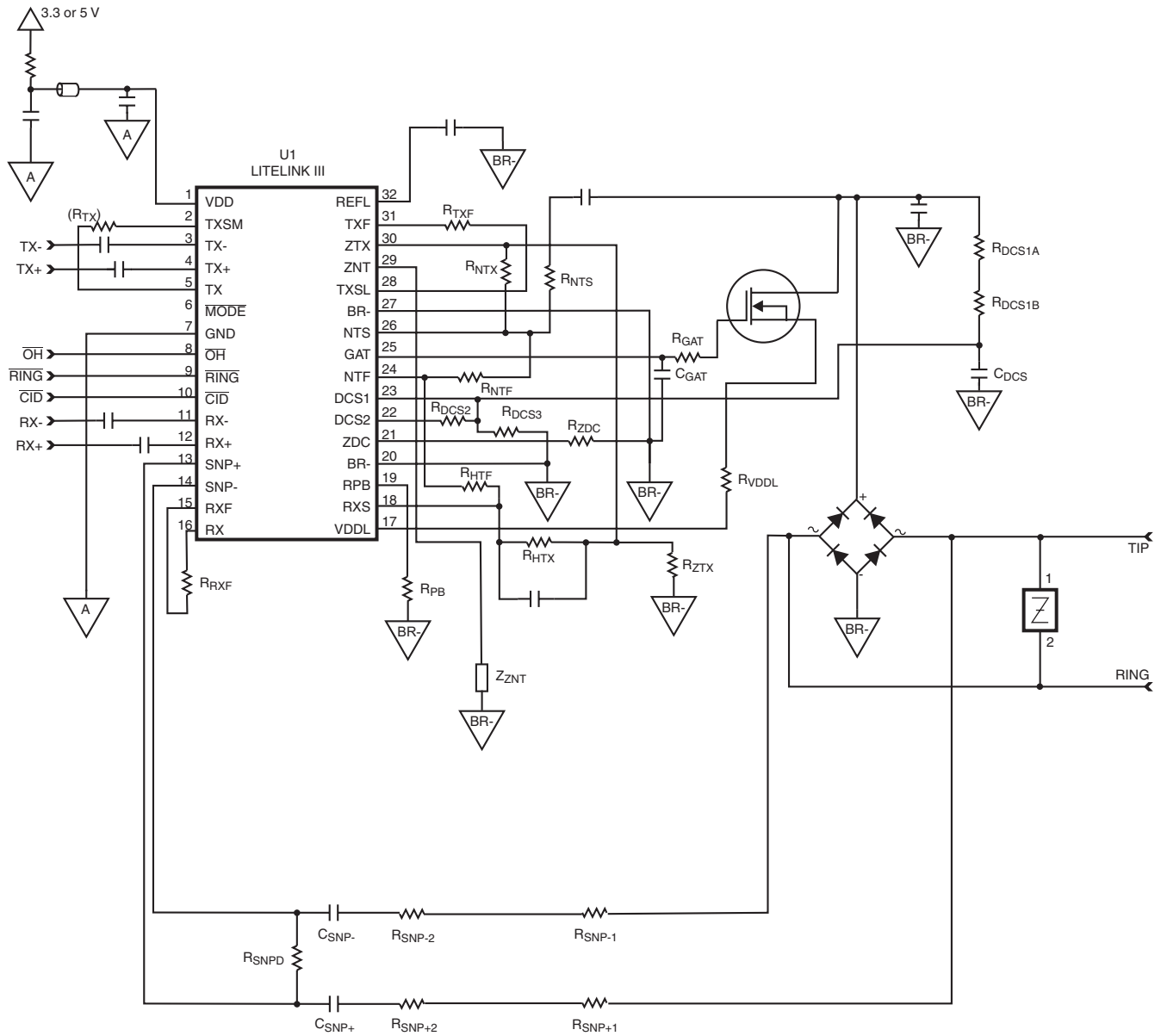
## 1. Introduction

Clare strongly recommends using the application circuits provided in LITELINK III (CPC5620 and CPC5621) datasheet and application notes. These circuits have been designed and tested to comply with applicable regulatory requirements. It is possible, however, to adjust the values of certain application circuit components to achieve specific results.

This application note provides the equations used by Clare engineers to arrive at the recommended application circuit values. With this information you will be able to make slight adjustments. Changes to the provided recommendations may yield an application circuit that does not meet safety and other regulatory or performance requirements.

Mnemonics in the equations refer to components in the standard LITELINK III application circuit shown in [Figure 1](#).

**Figure 1. LITELINK III Resistive Termination Circuit**



## 2. LITELINK III DC Characteristic Equations

The following equations describe the dc operating characteristics of the telephone line side of LITELINK III and LITELINK III dc requirements for the loop.

### 2.1 Loop Current Limit

$R_{ZDC}$ ,  $R_{ZTX}$ , and  $R_{ZNT}$  determine the off-hook loop current.

Adjust the value of  $R_{ZDC}$  to modify the loop current limit characteristics.

$$I_{CL} = \left[ \frac{1V}{R_{ZDC}} \right] + \frac{0.625V}{R_{ZTX} \parallel R_{ZNT}} + 5.5mA$$

### 2.2 Minimum Line Operating Current

The portion of the LITELINK on the telephone line side of the internal optical barrier is powered from the phone line, and requires a minimum operating current from the phone line to work. This value is calculated as follows:

$$I_{MIN} = \frac{0.625V}{R_{ZTX} \parallel R_{ZNT}} + 5.5mA$$

## 2.3 DC Line Current Versus Line Voltage Characteristics

### 2.3.1 Minimum Loop Voltage

The minimum loop voltage with which LITELINK III will operate is defined as:

$$V_{LINE} \geq V_{BRIDGE} + V_{PEAK} + 3.25V$$

where  $V_{PEAK}$  is the peak value of the signal on the line.

Note:  $R_{DCS3}$  is not needed in circuits where ratio constraint described above is met.  $R_{DCS3}$  is not used in Clare application circuits, where the error introduced is negligible.

### 2.3.2 Line Current Programming Resistor Ratio Requirement

LITELINK III requires the following circuit ratio for operation:

$$\frac{R_{DCS1} \parallel R_{DCS3}}{(R_{DCS2} + R_{DCS1} \parallel R_{DCS3})} \approx \frac{1}{1.2}$$

Failure to meet this requirement will result in poor error cancellation within LITELINK III.

## 2.4 DC I-V With $R_{DCS3}$

The following equations describe loop current and voltage characteristics when  $R_{DCS3}$  is used and when the constraint in “**Line Current Programming Resistor Ratio Requirement**” on page 3 has been met.

$$I_{LINE} = \frac{\left[ (V_{LINE} - V_{BRIDGE}) \left( \frac{R_{DCS2} \parallel R_{DCS3}}{R_{DCS1} + R_{DCS2} \parallel R_{DCS3}} \right) \right] - 0.5V}{R_{ZDC}} + \frac{0.625V}{R_{ZTX} \parallel R_{ZNT}} + 5.5mA$$

$$V_{LINE} = V_{BRIDGE} + \left[ \frac{(R_{DCS1} + R_{DCS2} \parallel R_{DCS3})}{R_{DCS2} \parallel R_{DCS3}} \right] \left[ 0.5V + \left( I_{LINE} - \frac{0.625V}{R_{ZTX} \parallel R_{ZNT}} - 5.5mA \right) (R_{ZDC}) \right]$$

## 2.5 DC I-V Without $R_{DCS3}$

The following equations describe loop current and voltage characteristics when  $R_{DCS3}$  is not used and when the constraint in “**Line Current Programming Resistor Ratio Requirement**” on page 3 has been met.

$$I_{LINE} = \frac{\left[ (V_{LINE} - V_{BRIDGE}) \left( \frac{R_{DCS2}}{R_{DCS1} + R_{DCS2}} \right) \right] - 0.5V}{R_{ZDC}} + \frac{0.625V}{R_{ZTX} \parallel R_{ZNT}} + 5.5mA$$

$$V_{LINE} = V_{BRIDGE} + \left[ \frac{(R_{DCS1} + R_{DCS2})}{R_{DCS2}} \right] \left[ 0.5V + \left( I_{LINE} - \frac{0.625V}{R_{ZTX} \parallel R_{ZNT}} - 5.5mA \right) (R_{ZDC}) \right]$$

## 2.6 DC Line Current without $R_{DCS3}$ (in General)

The following equation describes loop current characteristics in general terms as used in the recommended Clare application circuit, where  $R_{DCS3}$

is not used and without regard to the constraint in “**Line Current Programming Resistor Ratio Requirement**” on page 3.

$$I_{LINE} = \frac{\frac{(V_{LINE} - V_{BRIDGE})(R_{DCS2})}{(R_{DCS1} + R_{DCS2})} - \frac{(1.2)(R_{DCS1})(0.5V)}{(R_{DCS1} + R_{DCS2})} + (V_{TH}) \left[ \frac{(1.2)(R_{DCS1})}{(R_{DCS1} + R_{DCS2})} - 1 \right]}{R_{ZDC} + (R_S) \left[ \frac{(1.2)(R_{DCS1})}{R_{DCS1} + R_{DCS2}} - 1 \right]} + \frac{0.625V}{R_{ZTX} \parallel R_{ZNT}} + 5.5mA$$

Where:

$V_{TH} \sim 0.7V (\pm 0.2V)$ , and where

$R_S \sim 6\Omega (\pm 2\Omega)$ .  $R_S$  is an on-chip resistance.

## 3. LITELINK III AC Characteristic Equations

### 3.1 Ring Detection Threshold

The Ring detector threshold describes the input condition at which the LITELINK III ring detector output will change states. Ring detection threshold and display feature (caller-ID) signal gain (see “[Display Feature Signal Gain](#)” on page 5) are areas where customization of the LITELINK III application circuits is supported by Clare, Inc. Ring detection threshold is determined by the following equation:

$$V_{RINGPK} = \left( \frac{750mV}{R_{SNPD}} \right) \left[ (2R_{SNP} + R_{SNPD})^2 + \frac{1}{[(\pi \cdot f_{RING})(C_{SNOOP})]^2} \right]^{1/2}$$

For more information on setting the ring detection threshold see the [LITELINK datasheets](#) and Clare application note spreadsheet [AN-117, Customize LITELINK Caller ID Gain and Ring Detect Voltage Threshold](#).

### 3.2 Display Feature Signal Gain

Display feature (caller-ID) signal gain and ring detection threshold (see “[Ring Detection Threshold](#)” on page 5) are areas where customization of the LITELINK III application circuits is supported by Clare, Inc. Display feature signal gain can be calculated for both differential and single-ended circuit applications using the following equations:

#### 3.2.1 Differential Display Feature Gain

Between RX+ and RX-.

$$GAIN_{CID} = \frac{6R_{SNPD}}{\left[ (2R_{SNP} + R_{SNPD}) + \frac{1}{[(\pi \cdot f_{CID})(C_{SNOOP})]^2} \right]^{1/2}}$$

Where  $R_{SNP+} = R_{SNP-} = R_{SNP}$

**3.2.2 Differential Display Feature Gain (dB)**

Between RX+ and RX-.

$$GAIN(dB)_{CID} = 20\log \left[ \frac{6R_{SNPD}}{\left[ (2R_{SNP} + R_{SNPD}) + \frac{1}{[(\pi \cdot f_{CID})(C_{SNOOP})]^2} \right]^{1/2}} \right]$$

**3.2.3 Single-ended Display Feature Gain**

Between RX+ and RX-.

$$GAIN_{CID} = \frac{3R_{SNPD}}{\left[ (2R_{SNP} + R_{SNPD}) + \frac{1}{[(\pi \cdot f_{CID})(C_{SNOOP})]^2} \right]^{1/2}}$$

Where  $R_{SNP+} = R_{SNP-} = R_{SNP}$

**3.2.4 Single-ended Display Feature Gain (dB)**

Between RX+ and RX-.

$$GAIN(dB)_{CID} = 20\log \left[ \frac{3R_{SNPD}}{\left[ (2R_{SNP} + R_{SNPD}) + \frac{1}{[(\pi \cdot f_{CID})(C_{SNOOP})]^2} \right]^{1/2}} \right]$$

For more information on setting the display feature gain see the [LITELINK datasheets](#) and Clare application note spreadsheet [AN-117, Customize LITELINK Caller ID Gain and Ring Detect Voltage Threshold](#).

**3.3 Termination Impedance**

The following equation represents the ac impedance on the telephone loop represented by LITELINK III. It defines the  $\Delta V/\Delta I$  of LITELINK III.

$$Z_{TERMINATION} = \left( \frac{R_{NTS}}{R_{NTF}} \right) (Z_{ZNT})$$

**3.4 Transmit Insertion Loss (4-Wire to 2-Wire)**

**3.4.1 DC Transmit Ratio Constraint**

$$R_{TXF} = (0.749)(R_{TX})$$

The following circuit constraint must be met for correct operation of LITELINK III.

### 3.4.2 Insertion Loss to Line

LITELINK III transmit gain can be calculated as:

$$GAIN_{TX} = \left(\frac{1}{1.5}\right) \left(\frac{R_{TXF}}{R_{TX}}\right) \left( \frac{\frac{Z_{ZNT} + R_{NTF}}{Z_{ZTX} + R_{NTX}}}{\frac{Z_{LINE} + R_{NTS}}{R_{NTS}}} \right)$$

LITELINK III transmit insertion loss (in decibels) can be calculated as:

$$IL_{TX_{dB}} = -20 \log \left[ \left(\frac{1}{1.5}\right) \left(\frac{R_{TXF}}{R_{TX}}\right) \left( \frac{\frac{Z_{ZNT} + R_{NTF}}{Z_{ZTX} + R_{NTX}}}{\frac{Z_{LINE} + R_{NTS}}{R_{NTS}}} \right) \right]$$

## 3.5 Receive Insertion Loss (2-Wire to 4-Wire)

### 3.5.1 DC Receive Ratio Constraint

The following circuit constraint must be met for correct operation of LITELINK III.

$$R_{RXF} = (1.30)(R_{HTX} \parallel R_{HTF})$$

### 3.5.2 Differential Insertion Loss to RX+/RX-

LITELINK III differential receive gain can be calculated as:

$$GAIN_{RX} = \left(\frac{2}{0.65}\right) \left(\frac{R_{NTF}}{R_{NTS}}\right) \left(\frac{R_{RXF}}{R_{HTF}}\right)$$

LITELINK III differential receive insertion loss (in decibels) can be calculated as:

$$IL_{RX_{dB}} = -20 \log \left[ \left(\frac{2}{0.65}\right) \left(\frac{R_{NTF}}{R_{NTS}}\right) \left(\frac{R_{RXF}}{R_{HTF}}\right) \right]$$

### 3.5.3 Single-ended Insertion Loss to RX+ or RX-

LITELINK III single-ended receive gain can be calculated as:

$$GAIN_{RX} = \left(\frac{1}{0.65}\right) \left(\frac{R_{NTF}}{R_{NTS}}\right) \left(\frac{R_{RXF}}{R_{HTF}}\right)$$

LITELINK III single-ended receive insertion loss (in decibels) can be calculated as:

$$IL_{RX_{dB}} = -20 \log \left[ \left(\frac{1}{0.65}\right) \left(\frac{R_{NTF}}{R_{NTS}}\right) \left(\frac{R_{RXF}}{R_{HTF}}\right) \right]$$

### 3.6 Trans-Hybrid Loss (4-Wire Return Loss)

The hybrid network is also known as the 2-to-4 wire converter. The loss from transmit path to receive path

is known as trans-hybrid loss, measured in decibels. LITELINK III trans-hybrid loss can be calculated as:

$$THL_{dB} = -20 \log \left[ \left( \frac{1}{0.65} \right) \left[ \left( \frac{1}{1.5} \right) \left( \frac{R_{RXF}}{R_{HTF}} \right) \left( \frac{R_{TXF}}{R_{TX}} \right) \left( 1 - \frac{R_{NTF}}{R_{NTX}} \right) + GAIN_{TX} \left( \frac{R_{NTF}}{R_{NTS}} \right) \left( \frac{R_{RXF}}{R_{HTX}} \right) \right] \right]$$

## 4. Reference Designations

The following table connects reference designators for circuit elements used in this application note with chip pin mnemonics. See also the schematic “LITELINK III Resistive Termination Circuit” on page 2.

Designator	Connects Pin	To
Z <sub>ZNT</sub>	ZNT	BR-
R <sub>NTF</sub>	NTF	pin NTS
Z <sub>ZTX</sub>	ZTX	BR-
R <sub>NTX</sub>	ZTX	pin NTS
R <sub>HTF</sub>	NTF	pin RXSL
R <sub>RXF</sub>	RX	pin RXF
R <sub>TXF</sub>	TXF	pin TXS
R <sub>TX</sub>	TX	pin TXSM
R <sub>ZDC</sub>	ZDC	BR-
R <sub>DCS1</sub>	BR+	pin DCS1
R <sub>DCS1</sub>	DCS1	pin DCS2
R <sub>DCS3</sub>	DCS1	BR-

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## 5. LITELINK Design Resources

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### 5.1 Clare, Inc. Design Resources

The Clare, Inc. web site has a wealth of information useful for designing with LITELINK, including application notes and reference designs that already meet all applicable regulatory requirements. LITELINK data sheets also contains additional application and design information. See the following links:

#### LITELINK datasheets and reference designs

Application note AN-117 **Customize Caller-ID Gain and Ring Detect Voltage Threshold for CPC5610/11**

Application note AN-141, **Enhanced Pulse Dialing with LITELINK**

Application note AN-146, **Guidelines for Effective LITELINK Designs**

Application note AN-152 **LITELINK II to LITELINK III Design Conversion**

Application note AN-155 **Understanding LITELINK Display Feature Signal Routing and Applications**

**For additional information please visit [www.clare.com](http://www.clare.com)**

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