V.22bis TBR-21 Embedded Modem
2430RD Designer's Guide

Rev. 1.0 March, 2001

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2430RD Reference Design Information

The Clare 2430RD reference material provides the necessary design information required to build a V22bis embedded socket modem for us with the North American telephone network.

Along with this Designers Guide, the 2430RD consists of the following information that is also available on Clare's website at www.clare.com .

1. 2430RD Designers Guide (PDF)
2. 2430RD Schematic Diagram (PDF)
3. 2430RD Schematic in PADS
4. 2430RD PCB Gerber Files
5. 2430RD Assembly Views (PDF)
6. EN55024 Test Report (PDF)
7. EN55022B, FCC15B, IC ES 003 Test Report
8. TBR-21 Test Report

Further information about the modem chip itself and the "AT" command set used in Clare's 2430RD design can be found on TDK Semiconductor's website at www.tsc.tdk.com .

Design Overview

The 2430RD reference design material provides the necessary information to manufacture a 2400bps embedded modem module for applications requiring a data communications link to the Public Switched Telephone Network (PSTN). Embedded Modem Modules (EMM) built using the 2430RD design information have been successfully tested for compliance to EN60950, EN55024, and TBR-21 to satisfy the requirements of many European applications. (Please refer to the 2420RD Designer's Guide for North American applications.)

The 2430RD modem module design produces a printed circuit board with dimensions of 1.45" x 1.85" (3.68cm x 4.70cm) that can be socketed or soldered into the host system controller board. OEMs can use the 2430RD to build embedded modem modules for a variety of low data rate applications such as a set top box billing modem or any remote data acquisition application. The 2430RD design supports a standard V.24 interface to the host Data Terminal Equipment (DTE).

Designed for Regulatory Compliance

- TBR-21 Compliance
- EN60950 Compliance
- EN55024 Compliance

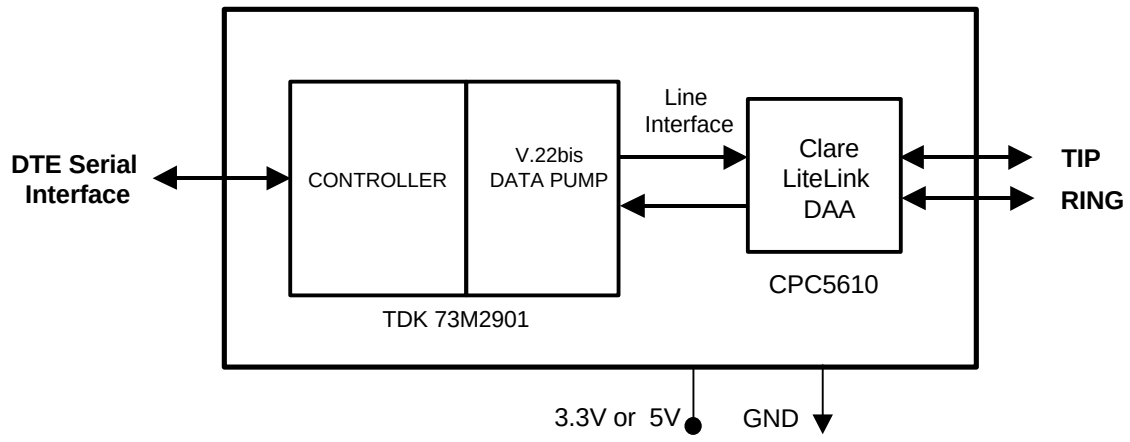
Design Features

- Full Duplex 2400bps Design
- Small 1.45" x 1.85" (3.68cm x 4.70cm) PCB
- Low Power Consumption and Sleep Mode
- V.24 DTE Interface
- 3.3V or 5.0V Operation
- Data Speed:
  - V.22bis – 2400bps
  - V.22, Bell 212 – 1200bps
  - V.21, Bell 103 – 300bps
  - V.23, Bell 1200/75bps
- Dynamic Range – 9dBm to –43dBm
- Caller ID Capability

Typical Applications Use of Design

- Vending / Gaming Machines
- Set Top Box Billing Modem
- Direct Broadcast Satellite
- Utility Meters
- Point of Sales Terminals
- Remote Diagnostics
- Remote Telemetry
- Remote Monitoring
- Embedded Applications

2430 Embedded Modem Functional Block Diagram



Modem Description

The 2430RD reference design architecture is based on a highly integrated TDK 73M2901 chip that includes the CPU, AFE, MAC, ROM, RAM, and UART that is controlled through the TDK "AT" like command set. Detailed information and support on this chipset can be found on the TDK Semiconductor website at www.tsc.tdk.com. The 2430RD EMM design also utilizes a compact Clare CPC5610 optical silicon DAA configured for TBR-21 European PSTN operation. The Clare CPC5610 DAA eliminates the on-board coupling transformer along with much of the regulatory agency certification risk usually associated with dial up modems. EMMs built using the 2430RD material have been successfully tested to be fully compliant with EN60950, EN55024, and TBR-21standards for interface to the telephone network. Clare's 2430RD EMM reference design is capable of being powered by either a single +3.3V or +5.0V power supply source and supports automatic standby idle mode. EMMs based upon the 2430RD will also accept a request to power down from the DTE via hardware control.

Low Power Mode

The 2430RD design supports a low power mode. If the low power standby option is enabled the modem module will go into a power saving mode when idle. The on board oscillator will be running, clocks will be supplied to the modem's UART, timers and interrupt blocks; but no clocks will be supplied to the CPU. Instruction processing and activity on the internal busses is halted. Normal operation is resumed when an interruption such as DTR, RING, or a character send to the modem occurs.

Asynchronous and Synchronous Serial Data Interface

The serial data interface consists of the TXD and RXD data paths (LSBit shifted in and out first, respectively); and the TXC and RXC serial clock outputs for synchronous data mode; CTS/RTS flow control; DCD, DSR and DTR. In synchronous mode, the data is passed at the bit rate (tolerance is +1%, -2.5%).

Important TBR-21 Operating Note

In order to be TBR-21 compliant, the following commands must be sent to the modem after Power Up Reset (POR):

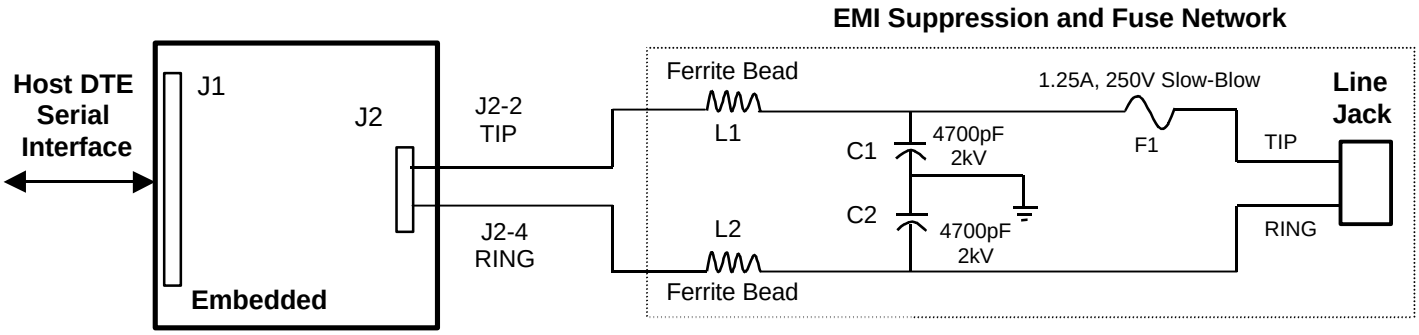
ATS99=0	Sets selection to TBR-21
ATS12=48	
ATS13=32	Adjust DTMF levels to be compliant to TBR-21

These commands must be issued before any other command. Do not issue an AT&F or ATZ command after the S registers have been set otherwise the default settings will be invoked and the unit will not be TBR-21 compliant.

Phone Line Interface

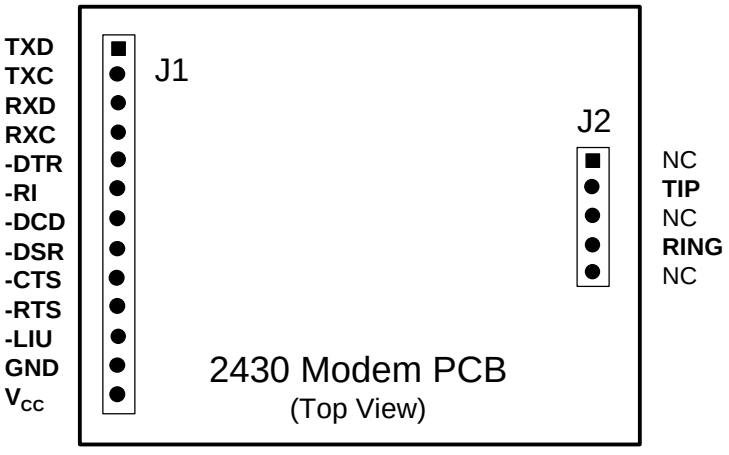
The 2430RD design connects to the telephone line via the TIP and RING pair of signal lines located on J2 of the EMM. An additional EMI suppression and fuse network connected to the TIP and RING signal lines is recommended.

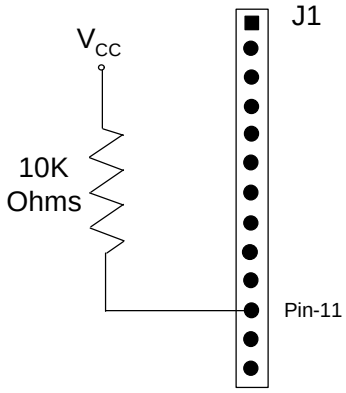
Recommended EMI Suppression and Fuse Network



PIN Definitions

PIN NAME	PIN NUMBER	I/O Type	Description
TXD	J1-1	I	Serial data input from DTE
TXC	J1-2	O	Transmit data synchronous clock
RXD	J1-3	O	Serial output to DTE
RXC	J1-4	O	Receive data synchronous clock
-DTR	J1-5	I	External interrupt - DTE DTR signal input
-RI	J1-6	O	Ring Indicator
-DCD	J1-7	O	Data Carrier Detect
-DSR	J1-8	O	Data Set Ready
-CTS	J1-9	O	Clear to Send
-RTS	J1-10	I	Request to Send
-LIU	J1-11	I/O	Line in Use
GND	J1-12	I	Connect to digital ground system
V_{CC}	J1-13	I	Positive supply voltage of 3.3V or 5.0V nominal
N.C.	J2-1	-	No connect
TIP	J2-2	I/O	To telephone line TIP connection via optional EMI suppression network and fuse.
N.C.	J2-3	-	No connect
RING	J2-4	I/O	To telephone line RING connection via optional EMI suppression network and fuse.
N.C.	J2-5	-	No Connection





If LIU is not used for "Line in Use" or "Parallel-Pick-Up" detection, it is advised to pull up Pin J1-11 as shown here:

Design Performance Parameters

Absolute Maximum Ratings (@ 25°C)

PARAMETER	MIN	MAX	UNITS
Isolation Voltage		1500	V_{RMS}
Tip/Ring Current	12	60	mA
Operating Temperature	-20	+85	°C
Storage Temperature	-40	+125	°C
Relative Humidity (Non-Condensing)	10	85	%
Soldering Duration			°C

DC Characteristics DTE Interface

(TXD, TXC, RXD, RXC, -DTR, -RI, DCD, -DSR, -CTS, -RTS, -LIU, GND, VCC)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Input Low voltage	V_{IL}	- 0.5	-	$0.2V_{CC}$	V	-
Input High voltage	V_{IH}	$0.5V_{CC}$	-	V_{CC} + 0.5	V	
Output Low voltage	V_{OL}	-	-	0.45	V	I_{OL} = 4mA
Output High voltage	V_{OH}	V_{CC} - 0.45	-	-	V	I_{OH} = -4mA
Input Leakage Current	I_{IH}	1	-	30	mA	$GND<V_{IN}< V_{CC}$

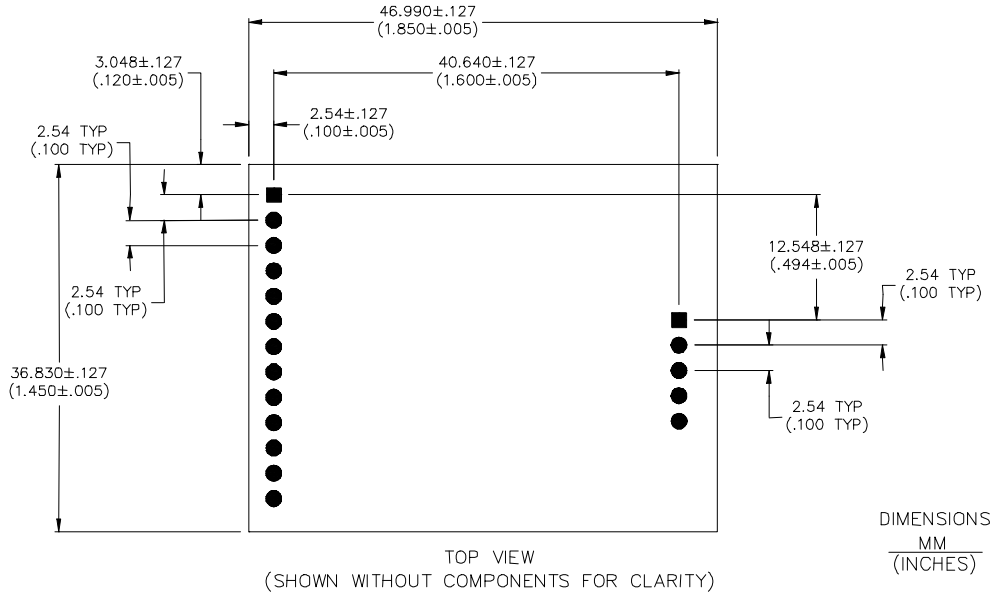
DC Characteristics 5V Operations

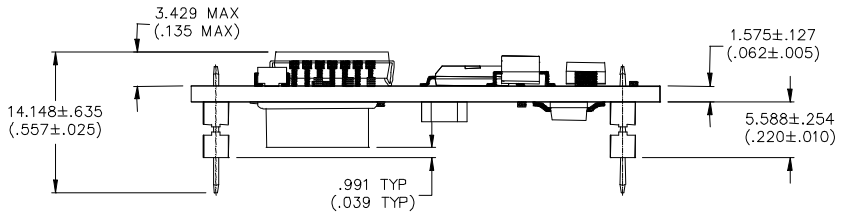
PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Max Power Supply Current	I_{DD11}		40.6		mA	Normal Mode
Max Power Supply Current	I_{DD2}		16.6		mA	Idle Mode
Max Power Supply Current	I_{DD3}	-	5.6		mA	Down Mode

DC Characteristics 3.3V Operations

PARAMETER	SYMBOL	MIN	TYP	MAX	UNIT	CONDITION
Max Power Supply Current	I_{DD11}		27.2		mA	Normal Mode
Max Power Supply Current	I_{DD2}		12.2		mA	Idle Mode
Max Power Supply Current	I_{DD3}	-	5.2		mA	Down Mode

Modem PCB Mechanical Dimensions





Bill of Materials

A complete list of the materials used in the 2430RD embedded modem reference design can be found below. The exact costs for the material will vary depending upon the quantities purchased and variable market conditions. In general, the material cost of the 2430RD should be under $8.00 US.

March, 2000 Rev.C

Clare 2430RD BOM
V.22bis (2400bps) TBR21 Embedded Modem Design

QTY	REF_DES	DEVICE	PKG	DESC	PKG_TYPE	VALUE	VOLT	WATT	TOL	VENDOR	VENDOR_PART_NO
9	C1-C4, C9,C15	CAPV_603	CHIP	CAP	CC0603	0.1	16V		10%	Tecate	CMC-016/104KX0603T
	C16,C18,C19										
2	C6-C7	CAPH_1808	CHIP	CAP	CC1808	220PF	2000V		10%	Nova Cap	1808N221K202NT
1	C10	CAPH_1206	CHIP	CAP	CC1206	0.01	500V		10%	Tecate	CMC-500/105JX1206T
1	C11	CAPV_603	CHIP	CAP	CC0805	0.027	16V		10%	Tecate	CMC-050/273JX0805T
1	C13	CAPV_603	CHIP	CAP	CC0603	27pF	50V		10%	Tecate	CMC-050/270JX0603T
1	C14	CAPV_603	CHIP	CAP	CC0603	33pF	50V		10%	Tecate	CMC-050/330JN0603T
3	C17, C20-C21	CAPV_3216	CHIP	CAP	3216	10	6.3V		10%	Tecate	522-016/100KTRB
1	C22			CAP	CC1812	.47uF	300V			Tecate	CMT-300/474MZ1812
1	DB1	SIZB60	BR_R	ECT	SHINDENBRI		600V			SHINDENGEN	SIZB60
1	J1	SIP-13P	CONN	13PIN	SIP-13P					Com Con Connectors	DS1-140/220/140-13G2
1	J2	SIP-5P	CONN	5PIN	SIP-5P					Com Con Connectors	DS1-140/220/140-05G2
1	Q1	CPC5602C	PWR	MOS	SOT223		350V			**CLARE**	**CPC5602**
4	R1,R2,R24,R26	RESV_603	CHIP	RES	CR0603	10K		1/16W	1%	Meritek	CR16103J
1	R3	RESV_603	CHIP	RES	CR0603	20k		1/16W	1%	Meritek	CR16203J
1	R4	RESH_603	CHIP	RES	CR0603	80.6K		1/16W	1%	IMS	RCI-0603-8062JT
1	R5	RESV_603	CHIP	RES	CR0603	127K		1/16W	1%	IMS	RCI-0603-1273JT
1	R6	RESV_603	CHIP	RES	CR0805	1.5M		1/16W	1%	IMS	RCI-0805-1504JT
2	R7,R8	RESH_603	CHIP	RES	CR0805	3.6M		1/10W	1%	IMS	RCI-0805-3604JT
1	R9	RESH_603	CHIP	RES	CR0603	42.2K		1/16W	1%	IMS	RCI-0603-4223FT
2	R10,R11	RESV_603	CHIP	RES	CR0603	1M		1/16W	1%	IMS	RCI-0603-1004JT
1	R12	RESV_603	CHIP	RES	CR0603	68.1		1/16W	1%	IMS	RCI-0603-68R1FT
1	R13	RESV_805	CHIP	RES	CR0805	22.1		1/8W	1%	IMS	RCI-0805-22R1FT
3	R14,R17,R27	RESH_603	CHIP	RES	CR0603	0		1/16W	1%	Meritek	CR16000J
2	R15,R16	RESH_603	CHIP	RES	CR0603	200K		1/16W	1%	Meritek	CR16204J
1	R18	RESH_603	CHIP	RES	CR0603	1.69M		1/16W	1%	IMS	RCI-0603-1694FT
1	R19	RESV_603	CHIP	RES	CR0603	4.7		1/16W	1%	IMS	RCI-0603-4R70JT
1	R20	RESV_603	CHIP	RES	CR1206	13M		1/4W	1%	IMS	RCI-1206-1305JT
1	R21	RESH_603	CHIP	RES	CR0603	270		1/16W	1%	IMS	RCI-0603-2700JT
1	R22	RESH_603	CHIP	RES	CR0603	150		1/16W	1%	IMS	RCI-0603-1500JT
1	R23	RESH_603	CHIP	RES	CR0603	300		1/16W	1%	IMS	RCI-0603-3000JT
1	R28	RESH_603	CHIP	RES	CR0603	150K		1/16W	1%	IMS	RCI-0603-1503JT
1	SP1	P3100SB	TRAN	SUPP	DO-214AA	350V				TECCOR	P3100SB
1	U1	CPC5610	DAA	IC	DIP32_SOL					**CLARE**	**CPC5610A**
1	U2	73M2901	DSP	IC						TDK	73M2901
1	Y1		XTAL	OSC		11.0592M				Ralton	AS-11.0592-18-Fund-Ext-SMD-T

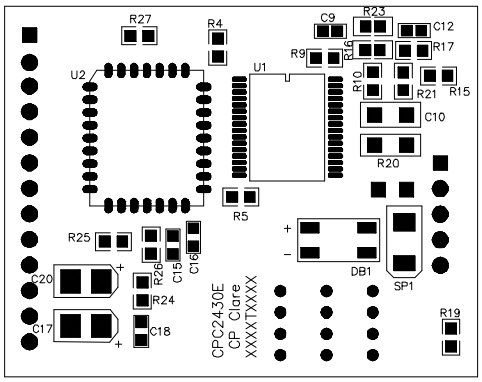
Assembly Figures

Basic PCB assembly drawings are shown below with further details available in the PCB files included as part of the 2430RD design package.

Assembly Instruction Notes:

1. Note orientation of U1, U2, C17, C20, and DB1
2. J1 and J2 are soldered on the bottom layer and soldered on the top layer
3. C8, C12, and R25 are not used

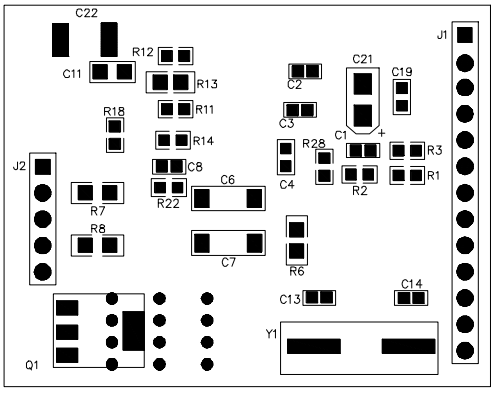
TOP LAYER ASSEMBLY INSTRUCTIONS



TOP LAYER

NOT USED
C12, R25

BOTTOM LAYER ASSEMBLY INSTRUCTIONS



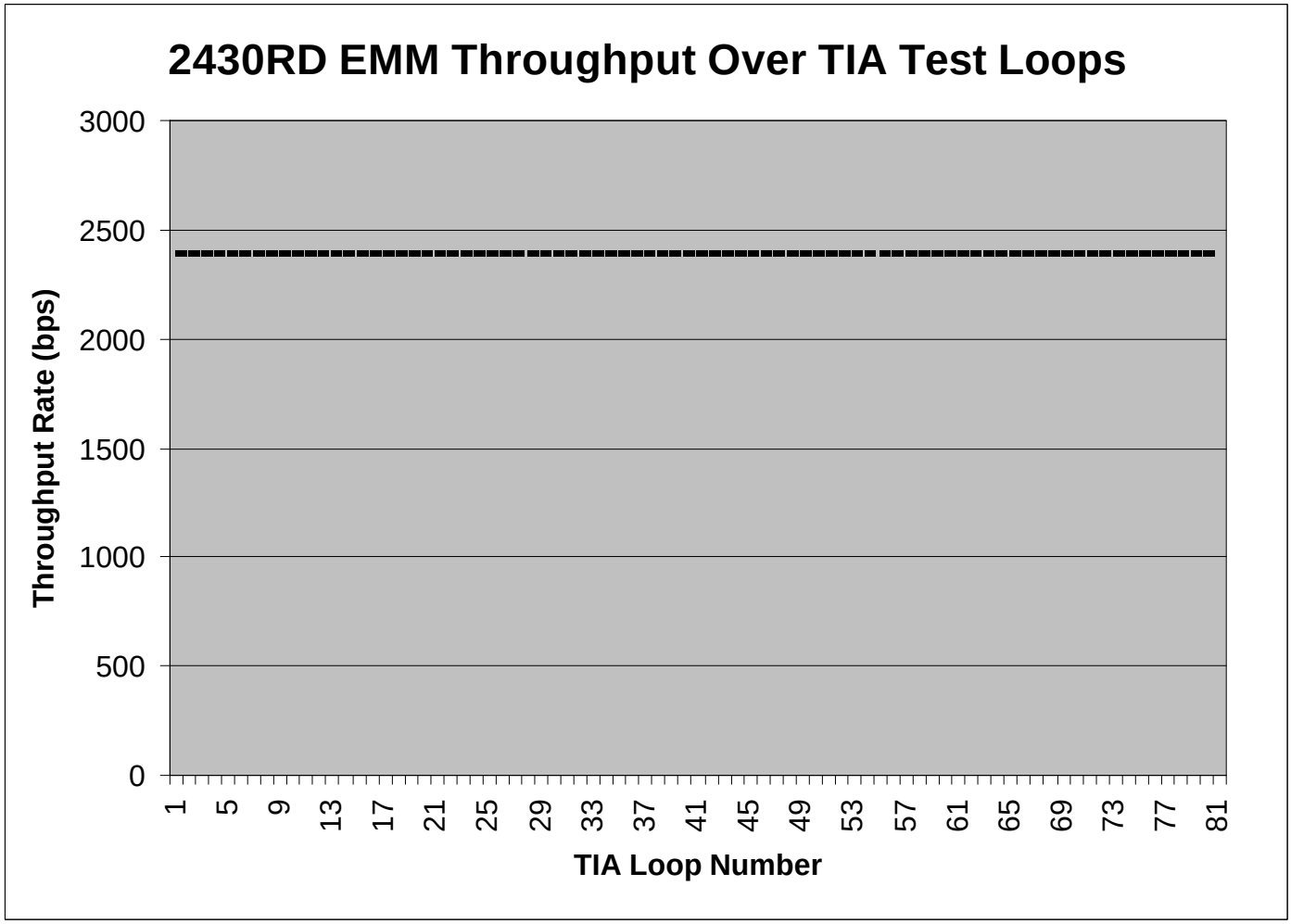
BOTTOM LAYER

NOT USED
C8

Performance Test Data

Clare has performed automated testing of embedded modems built using the 2430RD design material using TAS Telephone Network Emulators. The TAS Emulators test loops are compatible with the testing standards from the EIA/TIA, NTT, and RITT and incorporate built-in setup files for common exchange and impairment conditions. Each TAS Emulator test loop has been assigned a percentage of how often it occurs in the real world PSTN network allowing the TAS Emulator to be set up to perform many types of tests. Each loop is given an EIA and TIA identifier, for example our second line tested is the TIA case I9A, LoopB=EIA1. A good source for further information can be found in TIA document TR30.3, or the TAS web site www.taskit.com by going to the support pull down menu and then to application notes.

For modem designers, one of the more common tests performed is data throughput over the emulated PSTN test loops. Throughput testing checks the complete modem design by providing the initial connection speed information along with what the actual rate or throughput the data is transferred across the PSTN test loop. Therefore, TAS Emulator throughput test data provides information about the complete modem including the line interface or data access arrangement (DAA), the resolution of the codec, and most importantly the DSP's ability to compress and error correct the data. Data presented in the chart below represents the results Clare obtained form EMM built with the 2430RD design material. The actual raw test data can be found on the following page.



Test Loop	Description	Chars (B)	Chars/Sec (B)	Seconds (B)	% Complete (B)	Connect Response B
1	Clean case, Loop B = Null	131072	2.40E+02	546	100	2400
2	TIA case I9A, Loop B = EIA1	131072	2.40E+02	546	100	2400
3	TIA case I9A, Loop B = EIA3	131072	2.40E+02	546	100	2400
4	TIA case I9A, Loop B = EIA4	131072	2.40E+02	546	100	2400
5	TIA case I9A, Loop B = EIA5	131072	2.40E+02	546	100	2400
6	TIA case I9A, Loop B = EIA6	131072	2.40E+02	546	100	2400
7	TIA case I9B, Loop B = EIA1	131072	2.40E+02	546	100	2400
8	TIA case I9B, Loop B = EIA3	131072	2.40E+02	546	100	2400
9	TIA case I9B, Loop B = EIA4	131072	2.40E+02	546	100	2400
10	TIA case I9B, Loop B = EIA5	131072	2.40E+02	546	100	2400
11	TIA case I9B, Loop B = EIA6	131072	2.40E+02	546	100	2400
12	TIA case I9C, Loop B = EIA1	131072	2.40E+02	546	100	2400
13	TIA case I9C, Loop B = EIA3	131072	2.40E+02	546	100	2400
14	TIA case I9C, Loop B = EIA4	131072	2.40E+02	546	100	2400
15	TIA case I9C, Loop B = EIA5	131072	2.40E+02	546	100	2400
16	TIA case I9C, Loop B = EIA6	131072	2.40E+02	546	100	2400
17	TIA case I9D, Loop B = EIA1	131072	2.40E+02	546	100	2400
18	TIA case I9D, Loop B = EIA3	131072	2.40E+02	546	100	2400
19	TIA case I9D, Loop B = EIA4	131072	2.40E+02	546	100	2400
20	TIA case I9D, Loop B = EIA5	131072	2.40E+02	546	100	2400
21	TIA case I9D, Loop B = EIA6	131072	2.40E+02	546	100	2400
22	TIA case I10A, Loop B = EIA1	131072	2.40E+02	546	100	2400
23	TIA case I10A, Loop B = EIA3	131072	2.40E+02	546	100	2400
24	TIA case I10A, Loop B = EIA4	131072	2.40E+02	546	100	2400
25	TIA case I10A, Loop B = EIA5	131072	2.40E+02	546	100	2400
26	TIA case I10A, Loop B = EIA6	131072	2.40E+02	546	100	2400
27	TIA case I10B, Loop B = EIA1	131072	2.40E+02	546	100	2400
28	TIA case I10B, Loop B = EIA3	131072	2.40E+02	546	100	2400
29	TIA case I10B, Loop B = EIA4	131072	2.40E+02	546	100	2400
30	TIA case I10B, Loop B = EIA5	131072	2.40E+02	546	100	2400
31	TIA case I10B, Loop B = EIA6	131072	2.40E+02	546	100	2400
32	TIA case I10C, Loop B = EIA1	131072	2.40E+02	546	100	2400
33	TIA case I10C, Loop B = EIA3	131072	2.40E+02	546	100	2400
34	TIA case I10C, Loop B = EIA4	131072	2.40E+02	546	100	2400
35	TIA case I10C, Loop B = EIA5	131072	2.40E+02	546	100	2400
36	TIA case I10C, Loop B = EIA6	131072	2.40E+02	546	100	2400
37	TIA case I10D, Loop B = EIA1	131072	2.40E+02	546	100	2400
38	TIA case I10D, Loop B = EIA3	131072	2.40E+02	546	100	2400
39	TIA case I10D, Loop B = EIA4	131072	2.40E+02	546	100	2400
40	TIA case I10D, Loop B = EIA5	131072	2.40E+02	546	100	2400
41	TIA case I10D, Loop B = EIA6	131072	2.40E+02	546	100	2400
42	TIA case I11A, Loop B = EIA1	131072	2.40E+02	546	100	2400
43	TIA case I11A, Loop B = EIA3	131072	2.40E+02	546	100	2400
44	TIA case I11A, Loop B = EIA4	131072	2.40E+02	546	100	2400
45	TIA case I11A, Loop B = EIA5	131072	2.40E+02	546	100	2400
46	TIA case I11A, Loop B = EIA6	131072	2.40E+02	546	100	2400
47	TIA case I11B, Loop B = EIA1	131072	2.40E+02	546	100	2400
48	TIA case I11B, Loop B = EIA3	131072	2.40E+02	546	100	2400
49	TIA case I11B, Loop B = EIA4	131072	2.40E+02	546	100	2400
50	TIA case I11B, Loop B = EIA5	131072	2.40E+02	546	100	2400
51	TIA case I11B, Loop B = EIA6	131072	2.40E+02	546	100	2400
52	TIA case I11C, Loop B = EIA1	131072	2.40E+02	546	100	2400
53	TIA case I11C, Loop B = EIA3	131072	2.40E+02	546	100	2400
54	TIA case I11C, Loop B = EIA4	131072	2.40E+02	546	100	2400
55	TIA case I11C, Loop B = EIA5	131072	2.40E+02	546	100	2400
56	TIA case I11C, Loop B = EIA6	131072	2.40E+02	546	100	2400
57	TIA case I11D, Loop B = EIA1	131072	2.40E+02	546	100	2400
58	TIA case I11D, Loop B = EIA3	131072	2.40E+02	546	100	2400
59	TIA case I11D, Loop B = EIA4	131072	2.40E+02	546	100	2400
60	TIA case I11D, Loop B = EIA5	131072	2.40E+02	546	100	2400
61	TIA case I11D, Loop B = EIA6	131072	2.40E+02	546	100	2400
62	TIA case I12A, Loop B = EIA1	131072	2.40E+02	546	100	2400
63	TIA case I12A, Loop B = EIA3	131072	2.40E+02	546	100	2400
64	TIA case I12A, Loop B = EIA4	131072	2.40E+02	546	100	2400
65	TIA case I12A, Loop B = EIA5	131072	2.40E+02	546	100	2400
66	TIA case I12A, Loop B = EIA6	131072	2.40E+02	546	100	2400
67	TIA case I12B, Loop B = EIA1	131072	2.40E+02	546	100	2400
68	TIA case I12B, Loop B = EIA3	131072	2.40E+02	546	100	2400
69	TIA case I12B, Loop B = EIA4	131072	2.40E+02	546	100	2400
70	TIA case I12B, Loop B = EIA5	131072	2.40E+02	546	100	2400
71	TIA case I12B, Loop B = EIA6	131072	2.40E+02	546	100	2400
72	TIA case I12C, Loop B = EIA1	131072	2.40E+02	546	100	2400
73	TIA case I12C, Loop B = EIA3	131072	2.40E+02	546	100	2400
74	TIA case I12C, Loop B = EIA4	131072	2.40E+02	546	100	2400
75	TIA case I12C, Loop B = EIA5	131072	2.40E+02	546	100	2400
76	TIA case I12C, Loop B = EIA6	131072	2.40E+02	546	100	2400
77	TIA case I12D, Loop B = EIA1	131072	2.40E+02	546	100	2400
78	TIA case I12D, Loop B = EIA3	131072	2.40E+02	546	100	2400
79	TIA case I12D, Loop B = EIA4	131072	2.40E+02	546	100	2400
80	TIA case I12D, Loop B = EIA5	131072	2.40E+02	546	100	2400
81	TIA case I12D, Loop B = EIA6	131072	2.40E+02	546	100	2400

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